REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-8, 17 and 18 are pending in this case. Claims 1 and 2 are amended herein.

The Examiner rejected claims 1-3, 6, 7 17 and 18 under 35 U.S.C. § 102(e) as being anticipated by Saia et al. (U.S. Pat. No. 5,874,770).

Applicant respectfully submits that claim 1 is unanticipated by Saia et al as there is no disclosure or suggestion in Saia of a thin film resistor embedded within a multi-level dielectric layer between a lower metal interconnect layer and an upper metal interconnect layer, wherein the thin film resistor is physically separated in a vertical direction from any metal interconnect layer. Saia teaches a flexible interconnect film which includes a number of interconnect layers 21, 22, and those connected to 56, 52, etc. The resistor 28 is in contact interconnect 21. In contrast, the claim requires that the resistor is physically separated in a vertical direction from any metal interconnect layer. The claimed resistor is located between metal interconnect layers instead of at an interconnect layer and thus has the advantage of increased flexibility in designing the resistor since processes, materials, and chemicals do not have to satisfy the conditions of both the resistor and an interconnect layer. This is not disclosed or suggested by Saia. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Saia et al.

Applicant respectfully submits that claim 2 is further unanticipated by Saia et al as there is no disclosure or suggestion in Saia of a first via extending from the upper metal interconnect layer to the lower interconnect layer and a second via extending from the upper metal layer to the thin film resistor. No single via in

Saia extends from the upper m tal interconnect 56 to the lower metal interconnect 46 and no single via is taught as xtending from upper metal interconnect 56 to resistor 28.

Applicant respectfully submits that claim 17 is unanticipated by Saia as there is no disclosure or suggestion of the claimed thin film resistor in a semiconductor chip of an IC. Saia teaches a flexible interconnect film to which circuit chips 44 may be attached. Saia does not disclose or suggest a thin film resistor 28 as part of a semiconductor chip but rather as a part external to the circuit chip 44. Accordingly, Applicant respectfully submits that claims 17 and 18 are unanticipated by Saia.

Applicant respectfully submits that claim 18 is further unanticipated by Saia as there is no disclosure or suggestion in Saia of a first via extending from the upper metal interconnect layer to the lower interconnect layer and a second via extending from the upper metal layer to the thin film resistor. No single via in Saia extends from the upper metal interconnect 56 to the lower metal interconnect 46 and no single via is taught as extending from upper metal interconnect 56 to resistor 28.

The Examiner rejected claims 4, 5 and 8 under 35 U.S.C. §103(a) as being unpatentable over Saia et al. as applied to claim 1, and further in view of Linn et al. (U.S. Patent No. 5,547,896).

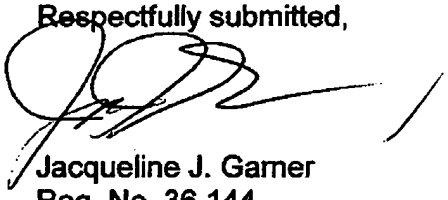
Applicant respectfully submits that claims 4, 5, and 8 are patentable over Saia in view of Linn for the same reasons discussed above relative to claim 1 from which these claims depend.

The Boyd reference cited by the Examiner has been reviewed but is not felt to come within the scope of the claims.

Attached hereto is a marked up version of the changes made to th specification and claims by the current amendm nt. The attached page is captioned "**Version with Markings to Show Changes Made.**"

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-8, 17, and 18. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



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V rsion with Markings to Show Changes Mad

1. (twice amended) An integrated circuit comprising:

a lower metal interconnect layer located over a semiconductor body;

a multi-level dielectric layer located over said lower interconnect layer;

an upper metal interconnect layer located over said multi-level dielectric layer; and

a thin film resistor embedded within said multi-level dielectric layer between [and physically separated in a vertical direction from] said lower metal interconnect layer and said upper metal interconnect layer, wherein said thin film resistor is physically separated in a vertical direction from any metal interconnect layer.

2. (amended) The integrated circuit of claim 1, further comprising:

a first [plurality of conductively filled vias] via extending from said upper metal interconnect layer to said lower interconnect layer; and

a second [plurality of conductively filled vias] via extending from said upper metal layer to said thin film resistor.